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Appl. No.: 10/709,690
Amdt. Dated: 10/28/2007
Reply to Office action of: 08/08/2007

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended) A distributed system for acquiring remote data in packets with a communication protocol optimizing the transmission speed, particularly applicable to the follow-up and control in an automotive vehicle of the values of signals provided by a series of transducer devices ~~(1, 2, 3, 4)~~ distributed in different parts of the vehicle and which follow different analog or digital values, characterized in that said transducer devices ~~(1, 2, 3, 4)~~ are associated to respective slave/subordinate circuits ~~(10, 20, 30, 40)~~ which are connected, through a single, time-shared serial communications bus ~~(60)~~, to a master/main circuit ~~(50)~~, which in turn is connected to a digital processing unit ~~(DP)~~ through a parallel bus ~~(70)~~, each one of said slave circuits ~~(10, 20, 30, 40)~~ and master circuit ~~(50)~~ being provided with a respective digital processor ~~(SLV1, SLV2, SLV3, SLV4, MST)~~ and a respective transceiver device ~~(11, 21, 31, 41, 51)~~, and which master circuit ~~(50)~~ is provided so as to perform, upon petition of an activation by said unit ~~(DP)~~, a repetitive or non-repetitive consultation, setting up communication with each one of the slave/subordinate circuits ~~(10, 20, 30, 40)~~ according to a communication protocol without error correction which includes a series of bit packets ~~(P1, P2, P3, P4)~~, each one of which comprises:

a start bit ~~(START)~~ with a longer duration/length than the data bits so that it is fully identified;

1.5 delay/synchronism bits ~~(SYNC)~~ for the frames going from master to slave;

one or more ~~(according to the number of slave devices present in the system)~~ address bits ~~(A1, A0)~~, indicative of the slave/subordinate circuit ~~device~~ ~~(10, 20, 30, 40)~~ to be consulted; and

several data bits ~~(D0...Dn)~~ containing information coming from the consulted slave/subordinate circuit ~~device~~ ~~(10, 20, 30, 40)~~.

Claim 2 (currently amended) A system according to claim 1, characterized in that said start bit ~~(START)~~ of each bit packet ~~(P1, P2, P3, P4)~~, with a longer duration/length than the data bits, is provided so as to generate a reinitialization of all the slave/subordinate circuits~~(10, 20, 30, 40)~~..

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Claim 3 (currently amended) A system according to claim 1, characterized in that said start bit ~~(START)~~ of each bit packet ~~(P1, P2, P3, P4)~~ has a duration of at least two times that of each one of the data bits of the packet.

Claim 4 (original) A system according to claim 1, characterized in that each bit of the packet in address, data or error detection functions, is encoded in Manchester format.

Claim 5 (currently amended) A system according to claim 1, characterized in that each bit packet ~~(P1, P2, P3,P4)~~ includes an additional protocol error detection bit ~~(DET)~~ in the data field or address field.

Claim 6 (currently amended) A system according to claim 5, characterized in that said error detection bit ~~(DET)~~ is the last one of each packet ~~(10, 20, 30, 40)~~.

Claim 7 (currently amended) A system according to claim 1, characterized in that ~~said~~ a short time interval ~~(t1)~~ of separation between bit packets ~~(P1, P2, P3, P4)~~ circulating through the serial bus ~~(60)~~ is comprised within a range of 0 to 1 bit.

Claim 8 (currently amended) A system according to claim 1, characterized in that said serial bus ~~(60)~~ is formed by a twisted differential cable comprising two twisted insulated copper conductors ~~(61, 62)~~ in shunt with a ground line ~~(64)~~.

Claim 9 (currently amended) A system according to claim 1, characterized in that said serial bus ~~(60)~~ is formed by a single insulated copper conductor ~~(63)~~ in shunt with a ground line ~~(64)~~.

Claim 10 (currently amended) A system according to claim 1, characterized in that each one of those transducer devices ~~(1, 2, 3, 4)~~ providing an analog signal is associated to an A/D converter ~~(12, 22, 32, 42)~~ connected to the corresponding ~~slave transceiver~~ slave/subordinate circuit transceiver ~~(SLV1-11, SLV2-21, SLV3-31, SLV4-41)~~.

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Claim 11 (currently amended) A system according to claim 1, characterized in that said digital processing unit ~~(DP)~~ is linked to another bus of the vehicle, such as a CAN or other type of bus.

Claim 12 (currently amended) A system according to claim 1, characterized in that each bit packet ~~(P1, P2, P3, P4)~~ contains, in addition to said one or more address bits ~~(A1, A0)~~, data bits ~~(10 ... 1n)~~ susceptible to being transmitted from the master circuit ~~(50)~~ to the consulted slave/subordinate circuit ~~(10, 20, 30, 40)~~, such that they are univocally recognized by said slave/subordinate circuits ~~the same~~.

Claim 13 (currently amended) A process for acquiring remote data in packets with a communication protocol optimizing the transmission speed, particularly applicable to the follow-up and control in an automotive vehicle of the values of signals provided by a series of transducer devices ~~(1, 2, 3, 4)~~ distributed in different parts of the vehicle and which follow different analog or digital values, integrated in a system according to claim 1, characterized in that:

said master circuit ~~(50)~~, upon petition of the application thereto of a signal ~~(wr)~~ emitted by said digital processing unit ~~(DP)~~, performs a repetitive or non-repetitive consultation of each one of the slave/subordinate circuits ~~(10, 20, 30, 40)~~ through the parallel bus ~~(70)~~, setting up communication with them through said time-shared serial bus ~~(60)~~ by means of said bit packets ~~(P1, P2, P3, P4)~~ according to said transmission protocol without error correction;

the slave/subordinate circuits ~~(10, 20, 30, 40)~~ transmit said data bits ~~(D1...Dn)~~ in response to said consultation, which data are stored in said master circuit ~~(50)~~ in arrayed entries;

the master circuit ~~(50)~~ sends an interruption order through a parallel bus ~~(70)~~, by means of the activation of a signal ~~(int)~~, to the digital processing unit ~~(DP)~~ indicative of the end of the consultation cycle; and

the digital processing unit ~~(DP)~~ acquires, by means of the activation of a reading order ~~(rd)~~, the data bits ~~(D1...Dn)~~ stored in the master circuit ~~(50)~~ while the system continues with a new consultation communication between the master circuit and the slave/subordinate circuits ~~(10, 20, 30, 40)~~.

Claim 14 (currently amended) A process according to claim 13, characterized in that said consultation cycles between master circuit ~~(50)~~ andslave/subordinate circuits ~~(10, 20, 30, 40)~~ and acquisition of data stored in the master circuit ~~(50)~~ from the digital processing unit ~~(DP)~~ are carried out cyclically at a predetermined frequency imposed by said digital processing unit ~~(DP)~~.

Claim 15 (currently amended) A process according to claim 13, characterized in that those bit packets ~~(P1, P2, P3, P4)~~ whose transmission has been detected as erroneous by means of said error detection bit ~~(DET)~~ are skipped over, passing to the next bit packets ~~(P1, P2, P3, P4)~~.